METHOD, APPARATUS AND COMPUTER PROGRAM PRODUCT FOR IMPLEMENTING AUTOMATED DETECTION OF EXCESS AGGRESSOR SHAPE CAPACITANCE COUPLING IN PRINTED CIRCUIT BOARD LAYOUTS

Field of the Invention

The present invention relates generally to the electronic design automation field, and more particularly, relates to a method, apparatus and computer program product for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts.

Description of the Related Art

As used in the present specification and claims, the term printed circuit board or PCB means a substrate or multiple layers (multi-layer) of substrates used to electrically attach electrical components and should be understood to generally include circuit cards, printed circuit cards, backplanes, printed wiring cards, printed wiring boards, flex circuits, and ceramic or organic chip packaging substrates.

In the layout of printed circuit boards typically including multiple layers or planes, a significant problem results from undetected capacitive coupling of electrical noise between an aggressor power plane or shape that generates noise and a victim shape that receives noise. A shape can be defined as a width or area of copper on a printed circuit board, potentially smaller than adjacent planes on the card, often used for power distribution or noise isolation.

Noise coupling can occur between any two shapes or planes that have overlapping areas.

Decoupling capacitors can be employed to significantly reduce the noise on the victim shapes by coupling their voltage to a more stable reference, such as ground, but the vulnerable power shapes must first be detected. If left undetected and uncorrected, noise on these shapes can cause significant circuit malfunctions, and possibly undesired electromagnetic emissions, necessitating a redesign of the board, and resulting in project delays, schedule slips, and lost revenue.

The current method employed to detect these susceptible shapes is to manually (visually) examine an electronic representation of the circuit card layout in order to locate such shapes. This process is very time consuming, tedious, and prone to manual errors such as overlooking possible vulnerable shapes, or flagging shapes that should not be decoupled, such as signals.

A need exists for an effective mechanism for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts.

Summary of the Invention

A principal object of the present invention is to provide a method, apparatus and computer program product for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts. Other important objects of the present invention are to provide such method, apparatus and computer program product for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts substantially without negative effect and that overcome many of the disadvantages of prior art arrangements.

In brief, a method, apparatus and computer program product are provided for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts. A PCB design file containing an electronic representation of a printed circuit board design is received. A list of candidate shapes is identified. The candidate shapes are

disposed on layers adjacent to power planes. An effective capacitance coupling the candidate shapes to adjacent noise-generating voltage planes is calculated. A ratio of the calculated effective capacitance and a decoupling capacitance connecting the candidate shapes to a reference plane is determined.

In accordance with features of the invention, the PCB design file containing an electronic representation of a printed circuit board design includes shape data and text data that are extracted to produce a list of shapes' names, areas, locations and planes; and includes data defining thickness and a relative permittivity of the dielectric layers. The candidate shapes have an assigned name that indicates usage. The calculated effective capacitance is an inter-layer parallel-plate effective capacitance represented by:

$$Cpp = eA/D$$

Where,

A = Plane and candidate shape overlap area (Meter^2)
e = er*eo, where er represents relative permittivity
eo equals 8.854x10^-12 Farads/Meter; (permittivity of free space)
D = the distance (Meters) between the candidate shape and the adjacent plane.

Brief Description of the Drawings

The present invention together with the above and other objects and advantages may best be understood from the following detailed description of the preferred embodiments of the invention illustrated in the drawings, wherein:

FIGS. 1 and 2 are block diagram representations illustrating a computer system and operating system for implementing methods for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts in accordance with the preferred embodiment;

FIG. 3 is a flow chart illustrating exemplary steps for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts in accordance with the preferred embodiment; and

FIG. 4 is a block diagram illustrating a computer program product in accordance with the preferred embodiment.

Detailed Description of the Preferred Embodiments

Referring now to the drawings, in FIGS. 1 and 2 there is shown a computer system generally designated by the reference character 100 for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts in accordance with the preferred embodiment. Computer system 100 includes a main processor 102 or central processor unit (CPU) 102 coupled by a system bus 106 to a memory management unit (MMU) 108 and system memory including a dynamic random access memory (DRAM) 110, a nonvolatile random access memory (NVRAM) 112, and a flash memory 114. A mass storage interface 116 coupled to the system bus 106 and MMU 108 connects a direct access storage device (DASD) 118 and a CD-ROM drive 120 to the main processor 102. Computer system 100 includes a display interface 122 coupled to the system bus 106 and connected to a display 124.

Computer system 100 is shown in simplified form sufficient for understanding the present invention. The illustrated computer system 100 is not intended to imply architectural or functional limitations. The present invention can be used with various hardware implementations and systems and various other internal hardware devices, for example, multiple main processors.

As shown in FIG. 2, computer system 100 includes an operating system 130, an electronic package design program 132, an excess aggressor shape capacitance coupling detection program 134 of the preferred embodiment, and a user interface 136 for displaying identified lists of candidate shapes for user review.

In accordance with features of the preferred embodiment, a method is provided that rapidly and accurately screens original design data that represents a circuit board under examination. Through the excess aggressor shape capacitance coupling detection program 134, the locations of possible vulnerable or candidate shapes are determined. The effective capacitance coupling the possible vulnerable shapes to adjacent noise-generating planes is calculated. It is then determined if sufficient coupling exists between the victim shapes and an adjacent reference plane. The advantages of this method include greatly increased speed, accuracy, and repeatability in the examination of the design for vulnerable shapes. Automating the process of examining the design data file for these shapes eliminates the possibility of manual errors through oversights or application of incorrect screening criteria.

Referring now to FIG. 3, there are shown exemplary steps for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts in accordance with the preferred embodiment. An original PCB design file containing an electronic representation of a printed circuit board design is received as indicated in a block 300. The original PCB design file is, for example, a Cadence Allegro board (.brd) file, where Allegro is the computer-aided printed circuit board design software sold by Cadence Design Systems, Inc.

The original PCB design file is manipulated via the excess aggressor shape capacitance coupling detection program 134 to create voided shapes as indicated in a block 302, for example, implemented in SKILL code. The voided shapes represent the areas of the noise-generating shapes with the overlapping areas of adjacent plane vulnerable shapes geometrically subtracted (voided) from the potential noise-generating shapes. A voided shapes PCB file is generated as indicated in a block 304 and a list of candidate voltage shapes is produced from the voided shapes as indicated in a block 306. Known Cadence layout tools support the SKILL language, for example, used at block 302. The list of candidate voltage shapes produced at block 306 are shapes that lie on layers adjacent to power planes and have an assigned name that indicates their usage possibly for power distribution, for example, such as VddA, V1.5, and the like.

From the voided shapes PCB file generated at block 304, shape data and text data are extracted as indicated in a block 308. A list of shapes' names, areas, locations, and planes is generated as indicated in a block 310.

Similarly from the original PCB design file received at block 300, shape data and text data are extracted as indicated in a block 312. A list of shapes' names, areas, locations, and planes is generated as indicated in a block 314.

Then the shapes lists generated at block 310 and 314 are compared, for example, using practical extension and report language (PERL) code as indicated in a block 316. A list of changed shapes is generated as indicated in a block 318. This list includes the area differences between the original noise-generating planes at block 314, and the voided versions of these shapes at block 310 and thus allows overlap area and capacitance calculations to be performed.

Then the list of candidate shapes generated at block 306 and the list of changed shapes generated at block 318 are compared, the effective capacitance coupling the possible vulnerable shapes to adjacent noise-generating voltage planes is calculated, and a list is created, for example, using PERL code as indicated in a block 320. Next a determination is made if sufficient capacitance coupling of identified possible vulnerable candidate shapes to a reference plane is present that includes creating a ranked list of shape names, a ratio of parallel capacitance to decoupling capacitance, an area, and a location as indicated in a block 322.

The excess aggressor shape capacitance coupling detection program 134 uses this list of candidate shapes at block 306 and at block 320 calculates the overlapping area between these shapes, and possible adjacent aggressor power shapes or planes. The resulting list of overlap areas together with the thickness and permittivity (er) of the dielectric layers, also contained in the .brd file received at block 300, are used to calculate effective inter-layer parallel-plate capacitance at block 320, represented by the following formula:

$$Cpp = eA/D$$

Where,

A = Plane and candidate shape overlap area (Meter^2)
e = er*eo, where er represents relative permittivity
eo equals 8.854x10^-12 Farads/Meter; (permittivity of free space)
D = the distance (Meters) between the candidate shape and the adjacent plane.

The value of Cpp will then be compared to the amount of decoupling capacitance connected from the shape to a reference plane; the ratios of these two numbers will be sorted and listed for user review, along with shape net names and coordinates in the ranked list of shape names at block 322.

Referring now to FIG. 4, an article of manufacture or a computer program product 400 of the invention is illustrated. The computer program product 400 includes a recording medium 402, such as, a floppy disk, a high capacity read only memory in the form of an optically read compact disk or CD-ROM, a tape, a transmission type media such as a digital or analog communications link, or a similar computer program product. Recording medium 402 stores program means 404, 406, 408, 410 on the medium 402 for carrying out the methods for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts of the preferred embodiment in the system 100 of FIGS. 1 and 2.

A sequence of program instructions or a logical assembly of one or more interrelated modules defined by the recorded program means 404, 406, 408, 410, direct the computer system 100 for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board layouts of the preferred embodiment.

While the present invention has been described with reference to the details of the embodiments of the invention shown in the drawing, these details are not intended to limit the scope of the invention as claimed in the appended claims.